Novel 0.44μm² Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application

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Abstract

This paper describes the key technology to realize high density flash memory, which has quarter-micron Shallow Trench Isolation (STI), Ti-silicided polycrystalline silicon (poly-Si) gate and source/drain, and tungsten (W) local inter-connect sourceline. Extremely small cell size of 0.44μm² has been obtained with 0.25μm design rule. This cell size is about 30% reduction of conventional NOR flash cell. To minimize the cell size, the cell gate is patterned with length of 0.25μm, which can be achieved by using channel erasing scheme. STI and 0.15μm floating gate separation can realize a 0.55μm bitline pitch. W sourceline can reduce sourceline resistance and the number of metal sourcelines in the array. In addition, poly-Si gate and active source/drain areas are Ti-silicided at both cells and peripheral transistors, which results in high-speed operation of memory array and peripheral circuits. This high-density NOR cell technology will be essential to realize a low cost and high-performance flash memory and flash embedded logic devices.

Introduction

Recently, the demand for flash memories has increased as file and program memories for portable applications. Particularly, it is indispensable to reduce the bit cost and power consumption for these applications. In addition, flash memories embedded logic device have been getting much attention because of their high performance and flexibility for data and program change.

In this paper, we have realized novel high density NOR cell technology, which has quarter-micron STI, Ti-silicided poly-Si gate and source/drain, and W local inter-connect sourceline. This technology has been developed for low-cost and high-performance flash memories including embedded logic application.

Cell Structure

To achieve a low bit cost and high cell performance, three key technologies have been introduced. (1) Gate poly-Si and source/drain of the cell transistors are Ti-silicided. This silicided gate has low resistance, which enables high-speed operation. In addition, 0.25μm cell gate length is applied to the cell, which is shown in Fig.1(a). This gate length can be achieved by using such channel erasing schemes as ejecting electron from a floating gate to the substrate by Fowler-Nordheim (FN) tunneling. It is possible with this channel erasing scheme to make source diffusion layer shallower than that with conventional source erasing scheme, resulting in short cell gate length. (2) Shallow trench isolation with 0.3μm isolation space is applied to the cell[1]. This technique can realize 0.55μm bitline pitch with 0.15μm floating gate separation space[2], as shown in Fig.1(b). (3) Source diffusion layers have been connected to the W local inter-connect, as shown in Fig.2(a). The W local inter-connect is formed parallel to the wordline, from edge to edge of the memory cell array (about 500μm length). The number of metal sourcelines parallel to bitlines can be dramatically decreased due to low resistance of W inter-connect compared to conventional diffused sourceline with self-aligned source structure. Moreover, bitline contacts have a borderless structure in the active area using barrier SiN etching stopper. These key technologies accomplish the extremely small cell size of 0.44μm², as shown in Table 1.

Process Integration

The proposed flash memory has a conventional STI structure in the peripheral circuits, as compared with the memory cell array which has self-aligned STI structure[3]. Poly-Si gate and active source/drain areas are Ti-silicided at both cells and peripheral transistors areas.

The fabrication process flow of the proposed NOR flash device is outlined in Fig.3(a). After cell/high-voltage transis-

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tor well and tunnel oxide are formed, the active area is isolated by the STI formation using self-aligned mask of a poly-Si gate. Then, the floating gate space is formed with spacing of 0.15μm by the SiN spacer process[2]. After ONO inter-poly dielectric with 14nm effective oxide thickness are formed on the floating gate, the ONO and floating gate poly-Si of the peripheral area are removed. Next, low-voltage twin-well and both gate oxides of high/low voltage peripheral transistors are formed on the removed area. Then, 2nd poly-Si is deposited, which results in both the cell control gate and the peripheral gate. After gate patterning, SiN sidewall spacer is formed and the gate poly-Si and active source/drain area are Ti-silicided. After this salicidation process, barrier SiN layer is formed for etching stopper of borderless contacts. Finally, standard CMOS back-end process is followed[4]. It is noted that W local inter-connect technology is applied to the metal sourcelines in the memory cell arrays.

Device structure including peripheral transistors is shown in Fig.3(b). Peripheral high-performance CMOS transistors are realized using dual-gate salicide process with 0.25μm gate length and 5.5nm gate oxide, aiming at embedded logic and low power supply voltage applications. Adequate drain current has been obtained for both nMOS and pMOS transistors even at 1.8V operation, as shown in Table 2.

Memory Cell Characteristics

I_d-V_g characteristics of the cell transistor are shown in Fig.4. Gate punch-through is not shown at the gate length of 0.25μm. Moreover, no anomalous hump is observed in the subthreshold characteristic of the cell transistor. Figure 5 shows n^+ junction punch-through characteristics as a function of the isolation width. There is no punch-through between the bit-line contacts at the STI width down to 0.25μm. Cell program/erase characteristics are shown in Fig.6. In the proposed NOR cells, about 1μsec fast programming and 10msec erasing are achieved, as shown in the figures. The FN channel erasing scheme realized faster erasing time with low power consumption compared with source erasing scheme.

Endurance characteristics are shown in Fig.7. The threshold voltage window narrowing is small up to 10^5 program/erase cycles, as shown in Fig.7(a). Fig.7(b) shows the gate conductance degradation due to program/erase cycles. The degradation is small and also comparable to source erasing scheme up to 10^5 cycles. FN channel erasing scheme is suitable for future cells to reduce cell gate length maintaining high reliability of the cells.

ADM Characteristics

Figure 8 shows the threshold voltage (V_{th}) distribution of 64kbyte array diagonal memory (ADM) cell array in one program and one erase pulse after 10^0 and 10^4 program/erase cycles. A tight distribution is realized through the programming and erasing by one pulse without verification, because of good uniformity of the channel width and the coupling ratio in the memory cell. This is mainly due to using the self-aligned STI structure. Tight erased V_{th} distribution can realize low word-line-boosted voltage for read operation and results in fast access time. Moreover, V_{th} distribution shift due to 300℃ 20hour bake test is small, as shown in Fig.8(a). This result shows that the proposed cell with 14nm ONO and 8nm tunnel oxide has good data retention characteristics.

Summary

In conclusion, we have developed a new technology to realize high-density and high-performance NOR flash memories with extremely small cell size of 0.44μm^2 with 0.25μm design rule. Excellent endurance characteristics, tight threshold voltage distribution and good reliability have been verified in 64kbyte ADM cell arrays. The proposed technology is also an attractive candidate for flash memory embedded logic applications.

Acknowledgments

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[2] K.Shimizu et al., IEEE Tech. Dig. of IEDM, 271(1997).
[3] Y.Takeuchi et al., Symp. on VLSI Tech., 102(1998).
[4] M.Inohara et al., Symp. on VLSI Tech., 64(1998).

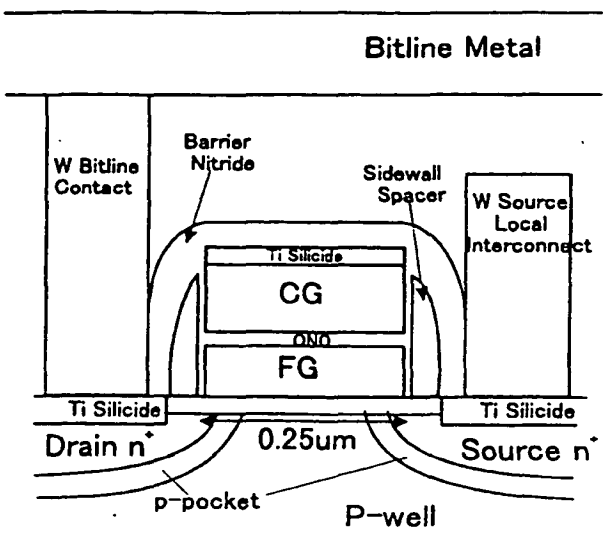
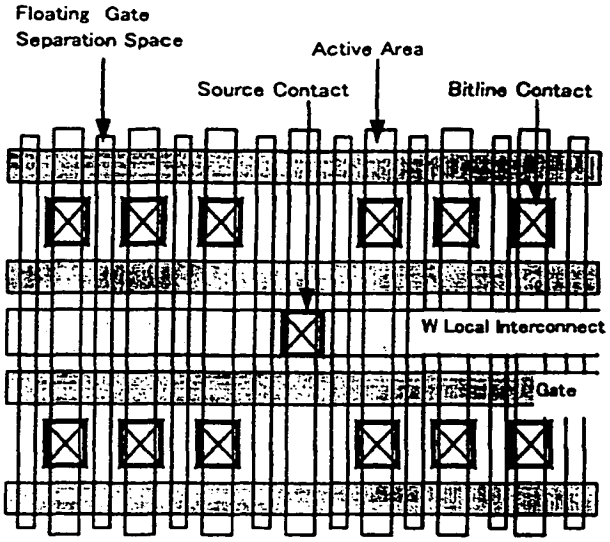


Fig.1 (a) Cross-sectional schematic view of the proposed NOR cell.



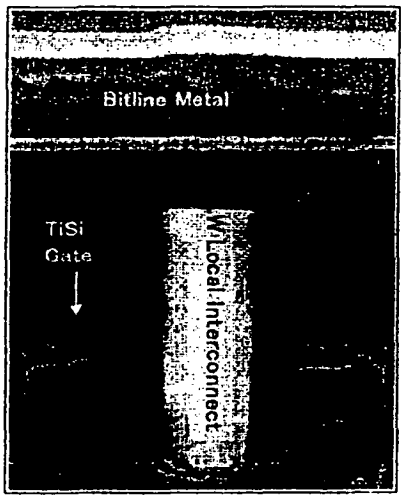
(b)Top schematic view of the proposed NOR cells.

Cell Size	0.55x0.80μm
Cell Gate Length	0.25μm
Cell Channel Width	0.25μm
Isolation Width	0.30μm
Floating Gate Separation	0.15μm
Source Line Width	0.30μm (W-LI)
Trench Depth	0.40μm
Tunnel Oxide	8.0nm
Interpoly ONO	14.0nm (effective)

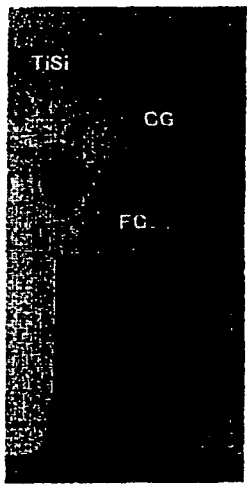
Table 1 Key process parameters of the cell design.

	I_{dr} (A/μm) @1.8V	poly-Si
PMOS	$1.25x10^{-4}$	n^+-poly
NMOS	$3.10x10^{-4}$	p^+-poly

Table 2 Device parameters of peripheral LV transistors at room temperature for 1.8V operation with 5.5nm gate oxide and 0.25μm gate length.



(a) Parallel to the bitline

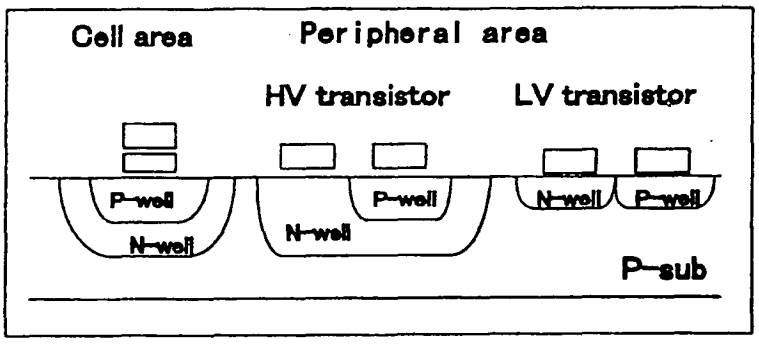


(b) Parallel to the wordline

Fig.2 Cross-sectional photographs of the proposed NOR cells: (a) parallel to the bitline (b) parallel to the wordline.

HV/Cell double well formation
Tunnel/Floating gate formation
STI process
ONO
Peripheral remove
LV twin well
Peripheral gate oxide
Gate definition
Salicide process
CMOS backend

(a) Process flow



(b) Device structure

Fig.3 (a) Process flow outline of the proposed NOR STI cells.
(b) Device structure schematic view of the NOR flash memories with dual-gate Ti-salicide.

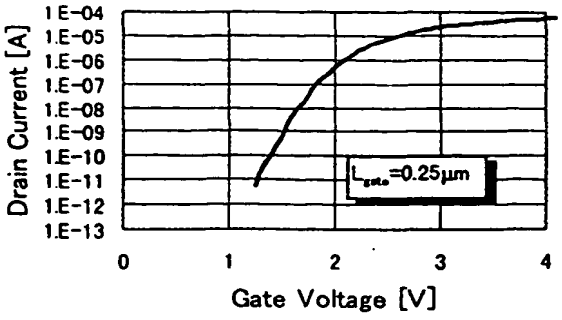


Fig.4 I_d-V_g Characteristic of the cell transistor. No anomalous hump is shown in the subthreshold characteristics.

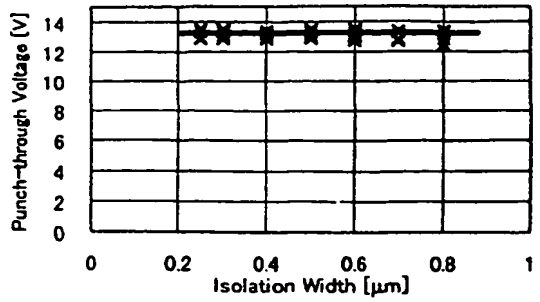
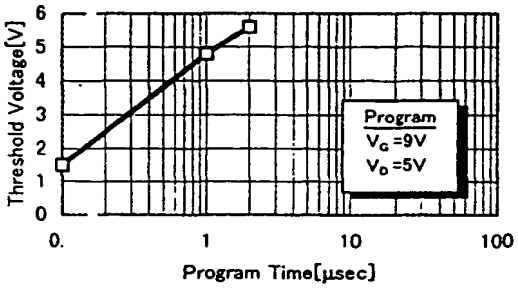
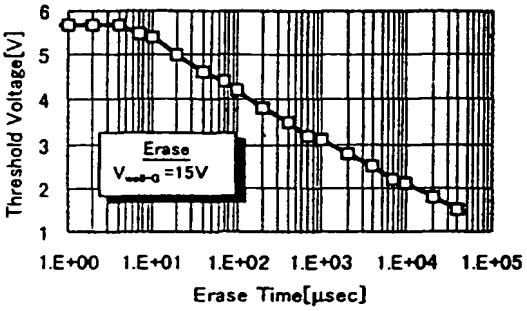


Fig.5 Punch-through voltage between the bitline n^+ junctions (without p-pocket structure). There is no punch-through at less than 12V up to 0.25μm.

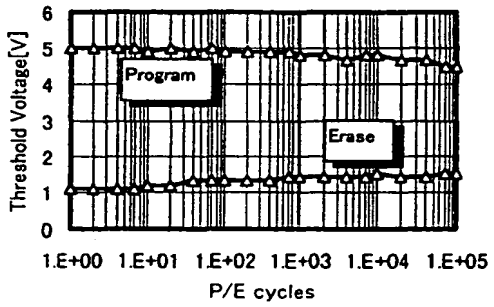


(a) Programming characteristics

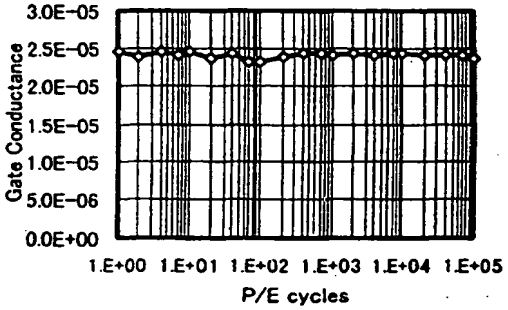


(b) Erasing characteristics

Fig.6 Program/Erase characteristics of the proposed NOR cell: (a) cell threshold voltage shift while programming, and (b) cell threshold voltage shift while erasing. Fast programming and erasing can be accomplished.

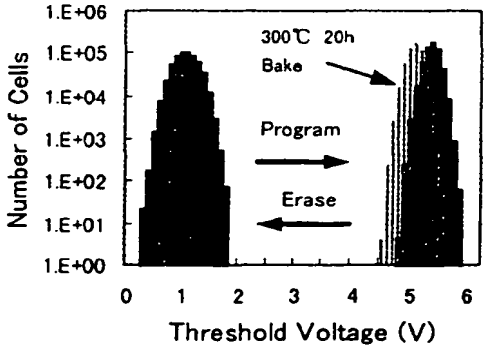


(a) Threshold voltage shift

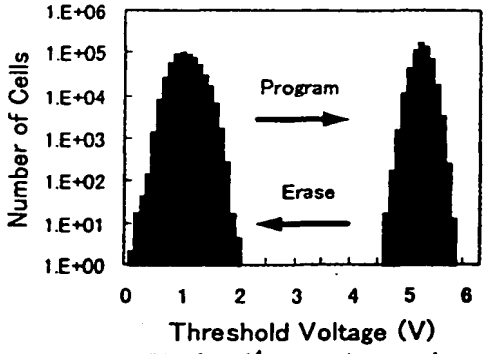


(b) Gate conductance shift

Fig.7 Endurance Characteristics of the NOR cell: (a) threshold voltage shift and (b) gate conductance shift. The threshold voltage window narrowing has not been clearly observed up to 10^5 cycles.



(a) Fresh device



(b) After 10^4 program/erase cycles

Fig.8 Threshold voltage distribution of the 64kbyte cell array in one program and one erase pulse (no verification) after (a) 10^0 program/erase cycles and (b) 10^4 program/erase cycles. Gray lines show the distribution after 300℃, 20hour bake.